AMENDMENTS TO THE SPECIFICATION

IN THE SPECIFICATION:

Please replace the paragraph [0043] on page 12 with the following rewritten paragraph:

[0043] In this embodiment, the first through twelfth transistors NV1, NV2, NI1-NI3, PV1, PV2, PI1-PI3, NR1 and NR2 are all NMOS transistors. Also, the transistors in a transistor group 52 connected to the pads PAD1 through PAD5 of the semiconductor device may have the same size as an NMOS transistor connected to the pad ~~(not shown)~~ PAD6 of a data input and/or output pin 30. Thus, the input capacitance for the pads PAD1 through PAD5 can be matched with that of the pad PAD6 of the data input and/or output pin.